REMARKS

Method claims 1-5 are now pending in this application. Claim 1 is independent. No claims have been amended or added by this amendment; claims 6-18 have been canceled by this Amendment.

Comments on Restriction

Claims 6-18, previously withdrawn as being directed to the non-elected testing structure, have been canceled by this amendment without prejudice or disclaimer. Applicants reserve the right to timely file a Divisional Application directed to the non-elected invention of claims 6-18.

Unpatentability Rejection

Withdrawal of the rejection of claims 1-5 under 35 U.S.C. §103(a) as being unpatentable over Yanof et al. (US 5,513,430) is requested.

At the outset, Applicant notes that, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, ***the prior art reference must teach or suggest all the claim limitations***.[1] Further, the teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, not in applicant's disclosure.[2]

Even assuming, *arguendo*, that the Examiner has provided the proper motivation to modify the single reference applied in this unpatentability rejection, the applied art does not teach or suggest all the claimed limitations.

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[1] *See* MPEP §2143.
[2] *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991) and *See* MPEP §2143.

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Yanof et al.

Yanof et al. is directed to a method for manufacturing a probe which can be used to test integrated devices using tapered or angled probes arranged at an acute angle to the pad to be tested. The tapered probes are configured to be compliant in both normal and lateral directions to accommodate pads of differing height without buckling (see, e.g., col. 5, lines 51-65).

The Examiner offers Yanof et al. as teaching a method of making a probe for testing semiconductor chips wherein passages are provided in a substrate, wherein electrically conducting material, e.g., metal, is provided in the plurality of passages. The Examiner also refers to metal filled vias 14 in FIG. 3 of Yanof et al.

The Examiner also asserts in the official action at page 2 that "[i]t is held to...[be] obvious to provide that the substrate can be a thin film if indeed the substrate itself cannot be construed to be a thin film...[and that] a POSITA would provide that the passages in the substrate be such that they [are] arranged so that a pattern exists which corresponds to a pattern of external connections on a semiconductor device. Otherwise why make the testing probe[?]"

Further, it appears that the Examiner may also be attempting to assert that Yanof et al. anticipates the pending independent claim 1 by stating "[this] is not to concede that the document itself fails to teach each and every limitation recite[d] in Applicants' claimed invention (in claim 1)."

For the reasons discussed below, Applicants respectfully disagree with the Examiner's characterization of the applied art, in particular the reading of pending independent claim 1 onto the disclosure of Yanof et al.

Deficiencies of Yanof et al.

The applied art, taken alone or in combination, does not teach or suggest a method for forming a structure for testing external connections to semiconductor devices which includes,

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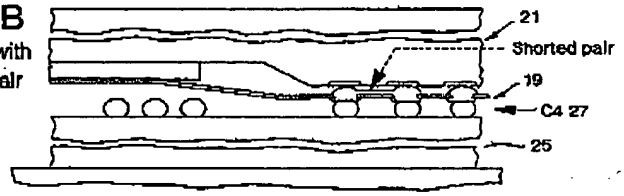
among other features, "...providing electrical connections ***between*** the electrically conducting material ***in selected passages***", as recited in original independent claim 1 (emphasis added).

As can be seen in FIG. 7B ("shorted pair") of the present application, and as discussed at least at paragraphs [0030], [0032], [0033], [0046], and [0047] of Patent Application Publication US 2004/0124867 A1 (corresponding to the present application, as originally filed), electrical connections are provided between selected passages to form one or more "shorted pairs".

FIG. 7B
TFI Probe with Shorted Pair



Advantages of Applicants' novel and non-obvious approach are also discussed at various places in the present Specification. These advantages include being able to quickly and efficiently conduct testing of external connections on semiconductor devices, including testing of C4 pads at the wafer level, and particularly including testing of pads by pairing adjacent I/O pads.

Notwithstanding whether or not the Examiner has provided an adequate basis for asserting that a POSITA would be motivated to modify Yanof et al. in the manner suggested, a proposition with which Applicants' disagree, the applied art clearly does not teach or suggest all the claimed limitations, as discussed above.

Accordingly, withdrawal of the explicit unpatentability rejection (and the apparent alternative anticipation rejection) and allowance of claims 1-5 are respectfully requested.

Conclusion

In view of the above distinguishing remarks and arguments, applicants believe that each of pending claims 1-5 in this application is in immediate condition for allowance.

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Applicant believes no fee is due with this response. However, if a fee is due, please charge IBM Deposit Account No. 09-0456, under Order No. 21806-00146-US1 from which the undersigned is authorized to draw.

Respectfully submitted,

By _____

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